

## **REMARKS**

Applicant thanks Examiner for the detailed review of the application. Applicant has amended claims 1, 2, 11-12, 14-15, 20-21, 25, 34-35, and 71-75. Applicant has cancelled claims 3-10, 13, 16-19, 22-24, 27-33, 36-70, 76-80.

### ***Specification***

The Office Action currently objects to applicant's specification for not including a Brief Summary of the Invention. Applicant has amended the specification to include a Brief Summary, as requested by The Office Action.

### ***Claim Objections***

The Office Action currently objects to applicant's claims 1, 2, 6, 9, 12, 35-37, 44, 49, 52, 55, 62, 69-72, and 79 because of informalities. Applicant has removed reference to IA-32. Furthermore, first reference to TLBVMX, such as in claim 71, has been initialed spelled out. Additionally, use of CPUID has been spelled out in claim 35.

### ***Claim Rejections -35 USC § 112***

The Office Action has rejected Claims 1, 2, 35, 36, 37, 70, 71, and 72, under 35 U.S.C. § 112(b) second paragraph for failing to particularly point out and distinctly claim the subject matter. Applicant has accordingly removed reference to IA-32.

### ***Claim Rejections -35 USC § 103(a)***

The Office Action has rejected Claims 1-19, 34-54, and 69-79 under 35 U.S.C. § 103(a) as being unpatentable over US Patent No.: 6,839,813 to Chauvel in view of US Patent No.: 6,674,536 to Long et al. (herein referred to as "Long")..

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is

only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has failed to meet one or more of these requirements.

Applicant's amended claim 1 includes, "a hardware **managed stack to hold a plurality of VMX mask word values** corresponding to a plurality of virtual machines (VMs), wherein a current VMX mask word value of the plurality of VMX mask word values, which corresponds to a current VM of the plurality of VMs, is to be utilized **to mask access by the current VM to a VMX control word**," (emphasis added). Chauvel only discloses invalidating entries based on a comparison of a qualifier (task ID or resource ID) of specified by a command with a qualifier in a field of the TLB entry (col. 10 lines 13-20). Furthermore, Chauvel states these resource IDs and task IDs are obtained from registers of a resource and/or task. However, Chauvel does not a hardware stack to hold mask values or that a current mask value masks access to that control word.

As described in applicant's detailed description in paragraph 0045, a hardware-managed stack to hold mask values, in one embodiment, supports layered virtualization. Therefore, different levels of access to a VMX control word may be provided for multiple layers of VMs through utilization of the stack and mask control word. In contrast, Chauvel's implementation allows for any resource or task to update the TLB utilizing a word format 400, which includes task ID field 402, resource ID field 404, and virtual address field 406. In addition to Chauvel, Long also does not disclose use of a mask control word or a hardware-managed stack.

Similarly, applicant's claim 71 includes, "a virtual machine extension (VMX) mask word to mask access to VMX control (TLBVMX) word during a VMX mode of operation." As stated

above, Chauvel only discloses invalidation of entries based on resource and/or task id fields associated with TLB entries. However, Chauvel does not describe **a mask word to mask access to a control word during a mode of operation**. In fact, by utilizing control word format 400, as described by Chauvel, any resource or task may operate on the TLB and update resource IDs and Task IDs of TLB entries accordingly. Furthermore, Chauvel does not describe one mode of operation, such as a VMX mode of operation, that a mask word is utilized to mask access to a control word.

As a result, applicant respectfully requests that independent claims 1 and 71, as well as their dependent claims, are now in condition for allowance for at least the reasons stated above.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,  
Intel Corporation

Dated: February 6, 2008

/David P. McAbee/Reg. No. 58,104/  
David P. McAbee  
Reg. No. 58,104

Intel Corporation  
M/S JF3-147  
2111 NE 25<sup>th</sup> Avenue  
Hillsboro, OR 97124  
Tele – 503-712-4988  
Fax – 503-264-1729